METHOD FOR MOUNTING CHIP

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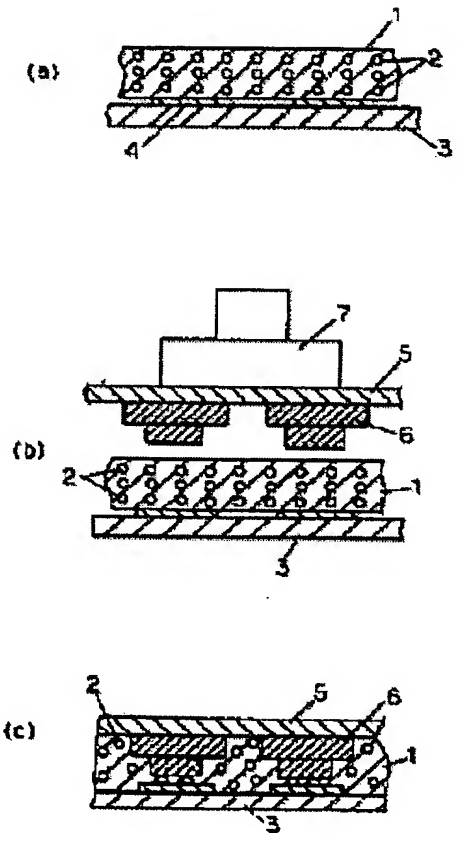
Abstract of **JP11026922**

PROBLEM TO BE SOLVED: To provide a method for mounting a chip with high connection reliability in which small pressure mounting and fluxless mounting can be attained. SOLUTION: A semiconductor chip 5 on which a gold bump 6 sucked by a tool 7 for ultrasonic pulse heat heating is formed is positioned on a substrate 3 on which an ACF1 is adhered, and pressurization is operated by adding an ultrasonic wave and pulse heat to the tool 7. Thus, the gold bump 6 and an electrode 4 are electrically connected by Ni particles 2 of conductive particles, and the gold bump 6 can be connected with the electrode 4 with a small pressure and fluxless by adding the ultrasonic wave to the tool 7.



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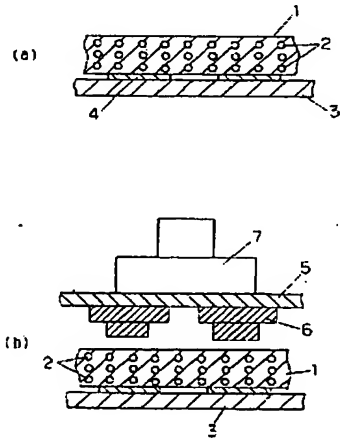
(54)【発明の名称】　チップ実装方法

(57)【要約】

【課題】　低荷重実装、フラックスレス実装を可能とし接合信頼性の高いチップ実装方法を提供することを目的とする。

【解決手段】　ＡＣＦ１を貼付した基板３に超音波パルスヒート加熱用のツール７で吸着した金バンプ６の形成された半導体チップ５を位置合わせし、ツール７に超音波とパルスヒートをかけながら加圧する。これにより金バンプ６と電極４は導電粒子であるＮｉ粒子２で電気的に接続される。ツール７に超音波を加えることにより、低荷重、フラックスレスで金バンプ６を電極４に接続できる。



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【特許請求の範囲】
【請求項1】バンプが形成されたチップを被接続母材に接続するための実装方法であって、バンプを母材に接続するために超音波を加えることを特徴とするチップ実装方法。
【請求項2】前記チップと前記被接続母材との間に異方性導電性接着剤を介して加熱するとともに加圧と超音波とをそれぞれ同時に加えて接続することを特徴とする請求項1記載のチップ実装方法。
【請求項3】前記バンプの材質は金、アルミニウム、ハンダのグループから選択された材質を用い、前記加圧に際しては1バンプ当たり5gから6gの範囲で加圧することを特徴とする請求項2記載のチップ実装方法。
【請求項4】ハンダを材質とするバンプが形成されたチップを被接続母材に接続するための実装方法であって、前記バンプと前記被接続母材とを位置合わせした状態で超音波を印加する加振ステップと、前記加振ステップの後に加熱し前記バンプと前記被接続母材とを溶融接続する加熱ステップと、前記加熱ステップの後に前記チップと前記被接続母材とを封止樹脂により結合する樹脂封止ステップとを有することを特徴とするチップ実装方法。
【請求項5】金を材質とするバンプが形成されたチップをハンダを材質とする被接続母材に接続するための実装方法であって、前記バンプと前記被接続母材とを位置合わせした状態で超音波を印加する加振ステップと、前記加振ステップの後に加熱し前記バンプと前記被接続母材とを溶融接続する加熱ステップと、前記加熱ステップの後に前記チップと前記被接続母材とを封止樹脂により結合する樹脂封止ステップとを有することを特徴とするチップ実装方法。
【請求項6】金を材質とするバンプが形成されたチップを表面に熱圧着硬化絶縁樹脂を有する被接続母材に接続するための実装方法であって、前記バンプと前記被接続母材とを位置合わせした状態で超音波を印加し前記熱圧着硬化絶縁樹脂を排除する加振ステップと、前記加振ステップの後に加熱して前記バンプと前記被接続母材とを接続するとともに排除された前記熱圧着硬化絶縁樹脂が硬化して前記チップと前記被接続母材とを結合する加熱ステップとを有することを特徴とするチップ実装方法。
【発明の詳細な説明】
【0001】
【発明の属する技術分野】本発明は、バンプ付き半導体チップを基板にフェースダウンで接続するためのチップ実装方法に関するものである。
【0002】
【従来の技術】バンプ付き半導体チップは、基板の小型化に有利なことから、各種コンピュータなどの多くの電子機器に多用されるようになってきている。バンプ付き半導体チップを基板に実装する方法として、従来より様々な方法が提案されている。
【0003】第1の方法は、ACF（異方性導電剤）を用いる方法である。この方法は、半導体チップと基板の間にACFを介在させ、半導体チップを加熱加圧することにより、ACFに混入された導電粒子によりバンプを基板の電極に接続するものである。
【0004】第2の方法は、バンプを半田により形成して半田バンプとし、リフローにより半田バンプを溶融固化させて基板の電極に接続するものである。この場合、半導体チップと基板の接合力を確保するために、好ましくは半導体チップと基板の間に封止用の樹脂が封入される。
【0005】第3の方法は、バンプを金により形成して金バンプとし、また基板の電極上にはメッキ等により半田をプリコートする。そして上記第2の方法と同様にリフローにより半田付けし、好ましくは封止用の樹脂を封入する。
【0006】第4の方法は、熱圧着硬化絶縁樹脂を用いる方法である。この方法は、基板に熱圧着硬化絶縁樹脂を塗布し、半導体チップの金バンプを基板の電極上に熱圧着し、熱圧着硬化絶縁樹脂を硬化させるものである。
【0007】
【発明が解決しようとする課題】しかしながら上記第1の方法では、Ni粒子などの導電粒子をバンプに食い込ませるために大きな荷重を半導体チップに加える必要があり、このため基板に大きなストレスが加わって回路パターンの断線を発生しやすく、また半導体チップもダメージを受けやすい。
【0008】また上記第2の方法は、リフローにより半田バンプを基板の電極に接着するため、荷重ストレスはほとんどないという利点がある。しかしながら第2の方法は半田のぬれ性を確保するためにフラックスを使用する必要があり、単にフラックス塗布やフラックス洗浄等の工程が必要となるだけでなく、フラックスを使用することによる環境上の問題が発生し、さらにはマイグレーションを引き起こしやすいなどの問題点がある。また樹脂封止を行った場合には、フラックスの残査により樹脂の封入時や硬化時に樹脂の流動性が阻害されてボイドが発生しやすくなり、ボイドが発生すると熱ストレスにより半田亀裂などの問題を誘発する。
【0009】また上記第3の方法も半田を用いることから、第2の方法と同様の問題がある。また第4の方法は、半導体チップに大きな荷重を加えねばならないため第1の方法と同様の問題がある。以上のように、従来方法は、いずれも様々な問題点を有していた。
【0010】そこで本発明は、上記従来の問題点を解決するもので、低荷重実装、フラックスレス実装を可能とし接合信頼性の高いチップ実装方法を提供することを目的としている。
【0011】
【課題を解決するための手段】本発明は、バンプ付き半

導体チップを基板の電極に実装する際に、超音波を加える実装方法とするものである。そしてこの方法により低荷重実装、フラックスレス実装が可能となり、接合信頼性の高いチップ実装方法が得られる。

【００１２】

【発明の実施の形態】請求項１から３に記載の発明は、バンプ付き半導体チップを基板の電極に実装する実装方法であって、異方性導電性接着剤を介し加熱・加圧・超音波を加えて実装する。この実装方法により、バンプを低荷重で基板の電極に接続させて実装することができる。

【００１３】請求項４および５に記載の発明は、バンプ側または基板の電極側のいずれかにハンダが使用されている場合の実装方法であって、超音波加振してハンダ表面の酸化膜を破壊し、加熱して溶融接合して樹脂封止する。この実装方法により、フラックスレスのハンダ接続を可能とし、信頼性の高い接合状態を得ることができる。

【００１４】請求項６に記載の発明は、熱圧着硬化絶縁樹脂を用いた実装方法であって、超音波加振し、加熱することにより熱圧着硬化絶縁樹脂を排除して電気的接続を行いり熱圧着硬化絶縁樹脂の硬化によりチップと基板とを結合する。この実装方法により、バンプを低荷重で基板の電極に接続させて実装することができる。

【００１５】（実施の形態１）図１は、本発明の実施の形態１のバンプ付き半導体チップの実装工程図であって、ＡＣＦによるフリップチップ実装に超音波を印加する場合の製造工程図を示すものである。

【００１６】図１において１はＡＣＦ、２はＮｉ粒子、３は基板、４は基板３上に形成された電極、５は半導体チップ、６は半導体チップ５に形成された金バンプ、７はツールである。次に実装方法を説明する。

【００１７】ＡＣＦ１の貼付が完了した基板３（図１（ａ））にツール７で吸着した金バンプ６の形成された半導体チップ５を位置合わせし（図１（ｂ））、ツール７に超音波とパルスヒートをかけながら加圧する（図１（ｃ））。

【００１８】この方法によれば、Ｎｉ粒子２が金バンプ６に捕獲後、超音波を加えながら加圧していくため、超音波の振動によりＮｉ粒子２はバンプ６と基板３上に形成された電極４に食い込み易くなる。従って、従来はＮｉ粒子２を金バンプ６に食い込ませるために１バンプ当たり５０～６０ｇの荷重を印加していたが、超音波によりＮｉ粒子２が金バンプ６及び基板３上に形成された電極４に食い込みやすくなるため、５ｇ～６ｇ（約１／５～１／６）の低荷重で接合が可能となる。また低荷重で半導体チップ５へのストレスも低減可能である。実際の超音波の印加方法は、超音波発信器を使用しツール７に超音波を印加し、超音波の方向はＡＣＦ１中のＮｉ粒子２を金バンプ６及び基板３上に形成された電極４に食い込ませるために各方向（Ｘ，Ｙ，Ｚ方向）併用しながら行う。

【００１９】またこの方法はＮｉ粒子を用いたＡＣＦのみならず、樹脂ボールに金メッキ、絶縁膜を施した導電粒子を用いたＡＣＦに対しても非常に有効である。通常、このタイプのＡＣＦは実装時に高荷重をかけ絶縁膜を破り押さえつけて電気的導通をとるが、ボンディング時に超音波を併用することにより、超音波が絶縁膜を破るため低荷重化を図ることができる。

【００２０】以上のことよりＡＣＦを用いた実装において超音波併用実装は非常に信頼性向上に有効な実装手段である。なお、超音波の印加方法はツールのみでなく、基板ステージから印加してもよく、また加熱においてもツール加熱ではなく、基板ステージからの加熱でもよい。さらに本実施の形態１ではパルスヒートツールを使用したが、常時加熱のコンスタント加熱でもよい。さらに本実施の形態１ではバンプ材質を金としているがバンプ材質に関しては金に限らず、半田、アルミ等他の金属にも適用される。

【００２１】（実施の形態２）図２は、本発明の実施の形態２のバンプ付き半導体チップの実装工程図であって、半田バンプを用いた実装方法を示すものである。図中、８は半導体チップ５に形成された半田バンプ、９は空気に触れることによりその表面に生じた酸化膜である。従来例で説明したように、半田バンプ８による実装では、実装荷重に関しては、基本的に基板３に低荷重（数ｇ／バンプ）で実装するため、基板３への荷重ストレスと言う点では特に大きな問題はないが、基板３上に形成された電極４への半田の濡れの向上、酸化膜９除去のために、従来はフラックスを使用していたものである。

【００２２】本方法では、実装時にツール７に超音波とパルスヒートをかけ実装する。具体的には、半田バンプ８の形成された半導体チップ５をまず基板３の電極４と位置合わせを行い実装する（図２（ａ））。次にツール７に半導体チップ５を吸着した状態で超音波をかける（図２（ｂ））。その結果、半田バンプ８と基板３上に形成された電極４とが超音波により擦れあい、酸化膜９が除去される。酸化膜９が除去された状態でツール７をパルスヒートにて加熱することにより半田バンプ８が溶融し、酸化膜９の無い部分において基板パターンに半田８が濡れ、良好な接合が得られる（図２（ｃ））。その後、半導体チップ５と基板３の間に封止樹脂１１を封入し、接合が完了する（図２（ｄ））。

【００２３】以上のことから半田接合においてフラックスレスが可能となり、洗浄工程が不要になる。さらにフラックス残査による封止樹脂１１の封入工程時の問題であったチップ基板間への封止樹脂１１の流れにくさによるボイドの発生の防止を図ることが可能で、信頼性が低下するといった問題が解消され、非常に信頼性の高い接

合状態を得ることが可能となる。なお、この実施の形態２では封止工程を半田バンプ８と基板３との接合が完了した後行っていたが、封止樹脂１１を実装時に同時にパルスヒートで硬化させる実装方式でもよい。

【００２４】（実施の形態３）図３は、本発明の実施の形態３のバンプ付き半導体チップの実装工程図であって、金バンプの形成された半導体チップを半田がプリコートされた基板に実装する方法を示している。図３において、１０は基板３の電極４上にメッキ法などによる半田である。この方法においても半田を使用するという特質上、従来は半田の基板上に形成された電極への濡れの向上、酸化膜の除去のためにフラックスを使用し実装していたものである。

【００２５】本方法では実装時にツール７に超音波とパルスヒートかけ実装する。具体的には、金バンプ６の形成された半導体チップ５をまず基板３の半田プリコートされた電極４と位置合わせを行い実装する（図３（ａ））。次にツール７に半導体チップ５を吸着した状態で超音波をかける（図３（ｂ））。その結果、金バンプ６と基板３上に形成された電極４に半田１０とが超音波により擦れあい、半田１０表面の酸化膜１１が除去される（図３（ｃ））。酸化膜９が除去された状態でツール７をパルスヒートにて加熱することにより基板３上に形成された電極４に半田１０が溶融し、酸化膜９の無い部分において金バンプ６表面に半田１０が濡れ、良好な接合が得られる。その後、封止樹脂１１で封止工程を行い接合が完了する（図３（ｄ））。

【００２６】以上のことから実施の形態２と同様な作用効果と同等の硬化が得られる。なお、この実施の形態３では封止工程をバンプと基板との接合が完了した後行っているが（図３（ｄ））、樹脂をボンディング時に同時にパルスヒートで硬化させる実装方式でもよい。

【００２７】（実施の形態４）図４は、本発明の実施の形態４のバンプ付き半導体チップの実装工程図であって、金バンプの形成されたチップを熱圧着硬化絶縁樹脂を用い基板に実装する方法を示している。具体的にはツール７に吸着された金バンプ６の形成された半導体チップ５を熱圧着硬化絶縁樹脂１２が塗布された基板３上の電極４に位置合わせし実装する（図４（ａ））。次にツール７に半導体チップ５を吸着した状態で超音波とパルスヒートをかける（図１（ｂ））。その結果、超音波により半導体チップ５形成された金バンプ６と基板３上に形成された電極４間の熱圧着硬化絶縁樹脂１２が周囲に排除され、金バンプ６表面と基板３上に形成された電極４の表面とが良好な接触が得られる。またパルスヒートによる加熱で熱圧着硬化絶縁樹脂１２が硬化し半導体チップ５と基板３とが固定される（図１（ｃ））。従って従来はバンプ基板の樹脂を排除するために高い荷重（約５０ｇ）をかけ実装していたが、超音波の併用により、低荷重（数ｇ　バンプ）での実装が可能であり、基板へのストレスも低減されかつチップへのストレスも低減される。

【００２８】

【発明の効果】以上のように本発明によれば、バンプ付き半導体チップを基板に実装する際に超音波を加えることにより、低荷重実装、フラックスレス実装が可能となり、接合信頼性の高い半導体チップの実装方法を実現できる。

【図面の簡単な説明】

【図１】本発明の実施の形態１のバンプ付き半導体チップの実装工程図

【図２】本発明の実施の形態２のバンプ付き半導体チップの実装工程図

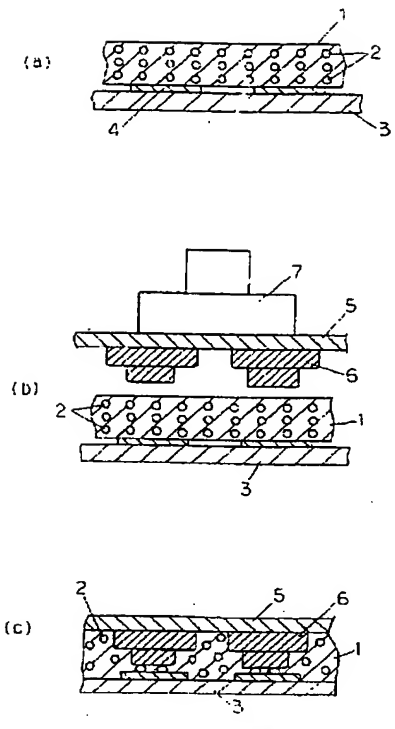
【図３】本発明の実施の形態３のバンプ付き半導体チップの実装工程図

【図４】本発明の実施の形態４のバンプ付き半導体チップの実装工程図

【符号の説明】

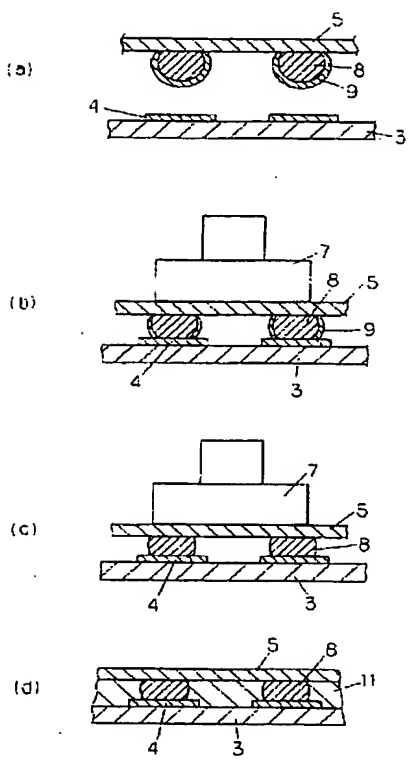
１　ＡＣＦ
２　Ｎｉ粒子
３　基板
４　電極
５　半導体チップ
６　金バンプ
７　ツール
８　半田バンプ
１０　半田
１１　封止樹脂
１２　熱圧着硬化絶縁樹脂

【図1】



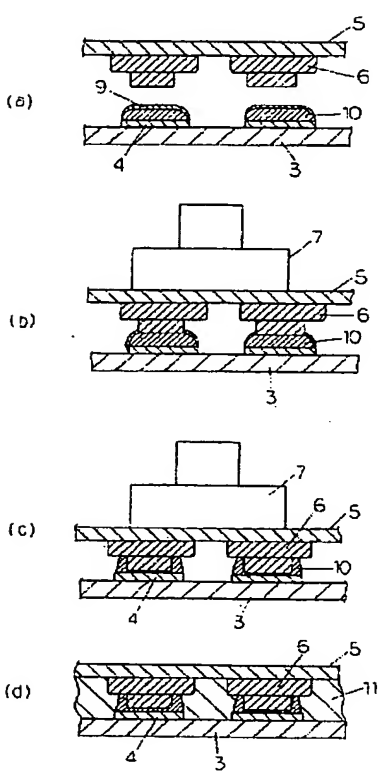
1　ACF
2　Ni粒子
3　基板
4　電極
5　半導体チップ
6　金バンプ
7　ツール

【図2】



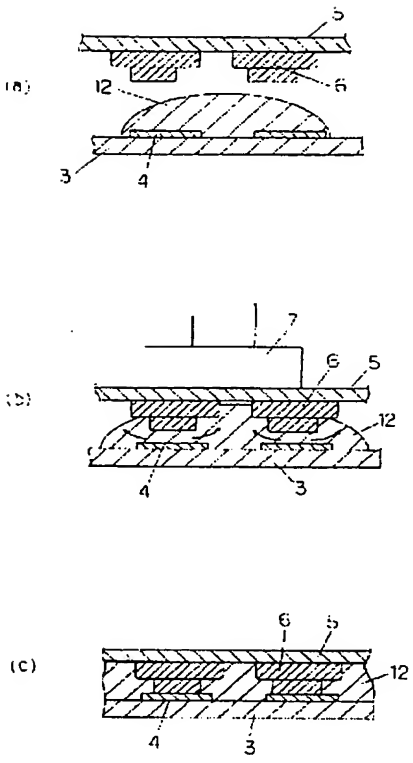
8　半田バンプ
11　封止樹脂

【図3】



10　半田

【図4】



12　熱圧着硬化絶縁樹脂

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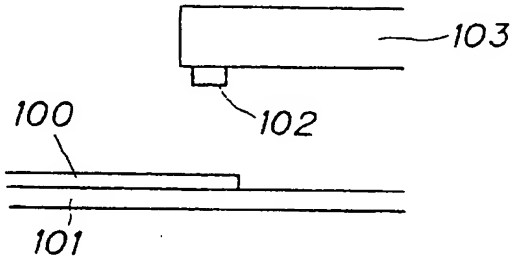
(54) **A structure of mounting a semiconductor element onto a substrate and a mounting method thereof**

(57) A semiconductor element/substrate mounting structure is formed by a first step of covering a resin film over the substrate together with a conductive portion; a second step of pressing and heating so that bumps penetrate through the resin film to come into contact with the conductive portion; and a third step of pressing and heating so that the bumps and the conductive portion become alloyed between the semiconductor element and the substrate.

FIG. 4A



EP 0 821 408 A2

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FIG.4B

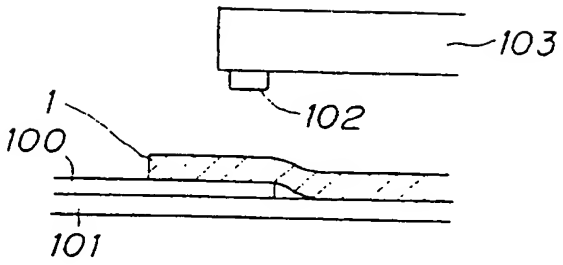


FIG.4C

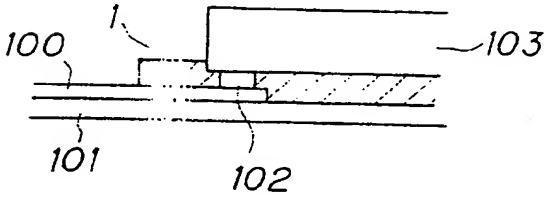
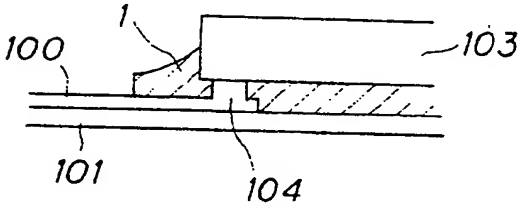


FIG.4D



Description

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a structure of mounting a semiconductor element onto a substrate and a mounting method thereof, and in particular relates to a structure of mounting a semiconductor element onto a substrate and a mounting method thereof wherein a semiconductor element (chip) having bumps is mounted to a conductive portion of a flexible substrate or the like.

(2) Description of the Prior Art

Referring to Figs.1A-1D, the prior art will be described. Figs.1A through 1D show procedural diagrams showing a mounting method of a semiconductor element of a conventional example.

Consider a case as shown in Fig.1A where a semiconductor chip 103 having bumps 102 consisting of gold is mounted to a flexible substrate 101 having a conductor pattern 100 as the conductive portion. Here, the surface of conductor pattern 100 is plated with tin. As to the number of the bumps, which corresponds to the number of terminals if the semiconductor chip is used as an IC, the chip has tens to hundreds of bumps, in general.

First, as shown in Fig.1B, the substrate and the chip are placed so that bumps 102 contact conductor pattern 100, and then they are heated and pressed to each other. This process is performed at a temperature of 280°C to 600°C, and each bump is about 100 μm square and is pressed with a load of 10 to 60 gf. As a result, bumps 102 and the tin plated on the surface of the conductor pattern, form an alloy layer 104 consisting of gold and tin, whereby semiconductor chip 103 is fixed and electrically connected to flexible substrate 101.

Next, as shown in Fig.1C, fluid resin 105 is applied between semiconductor chip 103 and flexible substrate 101 and also fills up the chip side, finally producing a mounted structure of the semiconductor chip as shown in Fig.1D.

Fig.2 is a sectional view showing a mounting structure of a semiconductor element in accordance with another conventional example. Components having the same functions are allotted with the same reference numerals as those in Figs.1A-1D. In this example, an anisotropic conductive film 107 with conductive particles 106 dispersed therein is applied onto the surface of a flexible substrate 101 with a conductor pattern 100 formed thereon. A semiconductor chip 103 having bumps 102 is pressed over this anisotropic conductive film 107 while being heated. Bumps 102 and conductor pattern 100 on flexible substrate 101 are electrically connected by conductive particles 106 within anisotropic conductive film 107. Semiconductor chip 103 and flexible substrate 101 are bonded by anisotropic conductive film 107 cured by heat.

The applied pressure in this case is similar to that in the case of Figs.1A-1D while the temperature causing formation of an alloy layer as in Figs.1A-1D is not needed but it is only necessary to cure anisotropic conductive film 107; this means that the temperature is set at about 200°C.

In the conventional example shown in Figs.1A-1D, electrical tests, etc., are implemented for the finished product as shown in Fig.1D. That is, the product is examined after alloy layer 104 has been formed between bumps 102 and conductor pattern 100 of flexible substrate 101, and resin 105 as filler has been applied. In this case, however, semiconductor chip 103 has already been fixed firmly to flexible substrate 101 by alloy layer 104.

Accordingly, if, from the electrical tests etc., semiconductor chip 103 turns out to be defective after the completion of the product, it is necessary to peel off conductor pattern 100 of flexible substrate 101 in order to remove the defective semiconductor chip 103. This means that flexible substrate 101 can not be reused, resulting in waste.

Further, in the heating step shown in Fig.1B where alloy layer 104 is formed, tin on the surface of conductor pattern 100 of flexible substrate 101 tends to gather toward bumps 102. As a result, there are cases where alloy layer 104 largely spreads further out from the joint area between a bump 102 of semiconductor chip 103 and conductor pattern 100. The thus formed alloy layer 104 directly comes in contact with other neighboring bumps or other conductor patterns, causing edge leakage.

Further, since this substrate is a flexible one, if substrate 101 becomes bent at a portion A encircled in Fig. 3, the overrun alloy layer 104 is liable to contact the end face of semiconductor chip 103.

In the mounting structure and mounting method shown in Fig.2, anisotropic conductive film 107 was used. However, conductive particles 106 can not always be dispersed uniformly within the film, conductive particles 106 may exist in relatively large densities at some places. These sites with a high particle density could cause damage to a circuit to be a joint area to semiconductor chip 103.

Further, conductive particles 106 should ideally function as electrical communication between bumps 102 and flexible substrate 101, but ununiformity of conductive particles 106 heightens the connection resistance, or causes unreliable connection, in the worst case, causing disconnection.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a mounting structure of a semiconductor element and a production method thereof wherein if a sem-

iconductor chip turns out to be defective after the completion of the product, it is possible to replace the defective chip so as to reuse the substrate and it is further possible to establish a reliable conduction without causing any edge leak problem, which occurred conventionally.

The present invention has been achieved to attain the above object, and the gist of the invention is as follows:

In accordance with the first aspect of the invention, a semiconductor element/substrate mounting structure of mounting a semiconductor element having bumps onto a conductor portion of a substrate via the bumps is characterized in that the bumps are alloyed so as to be integrated to the conductive portion on the substrate, the alloyed portion is formed penetrating through a resin film which is disposed so as to cover the substrate containing conductive portion.

In accordance with the second aspect of the invention, a semiconductor element/substrate mounting structure having the above first feature is characterized in that the substrate is of a flexible type.

In accordance with the third aspect of the invention, a semiconductor element/substrate mounting structure having the above first feature is characterized in that the resin film has characteristics which causes cross-linking at a temperature range within which the bumps and the conductive portion on the substrate become alloyed.

In accordance with the fourth aspect of the invention, a mounting method of a semiconductor element for mounting a semiconductor element having bumps so that the bumps are connected to a conductor portion of a substrate, includes:

a first step of covering a resin film over the substrate together with the conductive portion;
a second step of pressing and heating so that the bumps penetrate through the resin film to come into contact with the conductive portion; and
a third step of pressing and heating so that the bumps and the conductive portion become alloyed between the semiconductor element and the substrate.

In accordance with the fifth aspect of the invention, a mounting method of a semiconductor element having the above fourth feature is characterized in that the substrate is of a flexible type.

In accordance with the sixth aspect of the invention, a mounting method of a semiconductor element having the above fourth feature is characterized in that the resin film has such a characteristic that no cross-linking reaction occurs during the second step and a cross-linking reaction occurs to cure the resin film during the third step.

According to the configuration described above, electrical tests are adapted to have been already carried out before the bumps of the semiconductor element and the conductive portion of the substrate are alloyed. Therefore, when a semiconductor chip is judged as defective from the tests, only the defective semiconductor chip can be replaced easily so that the substrate itself can be reused. Therefore, it is possible to reduce waste as compared to the conventional configuration, thus providing a cost benefit.

Further, since each bump is surrounded by the resin film when an alloy layer is formed by pressing and heating, no phenomenon occurs in which tin plating on the surface of the conductor pattern gathers toward the bumps thereby forming an alloy layer spreading out from the end face of the semiconductor chip, as mentioned as a problem in the prior art. As a result, it is possible to solve the problem of edge leakage which occurred in the conventional configuration.

The above effects are more effective especially for a flexible substrate having flexibility.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs.1A-1D are diagrams showing procedural steps of mounting a semiconductor element onto a substrate in accordance with a conventional example;
Fig.2 is a sectional view showing a method of mounting a semiconductor element onto a substrate in accordance with another conventional example;
Fig.3 is a sectional view for illustrating the problems of the conventional example shown in Figs.1A-1D; and
Figs.4A-4D are diagrams showing procedural steps of mounting a semiconductor element onto a substrate in accordance with an embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

One embodiment of the present invention will hereinafter be described with reference to Figs.4A-4D. Fig. 4A through 4D are diagram showing procedural steps for illustrating a mounting method of a semiconductor element in accordance with this embodiment. Components having the same functions are allotted with the same reference numerals as those in the conventional example shown in Figs.1A-1D.

In this embodiment, as shown in Fig.4A, a semiconductor chip 103 having bumps 102 consisting of gold is mounted onto a flexible substrate 101 with a conductor pattern 100 formed thereon. The insulating material in this flexible substrate 101 is made from polyimide or polyester and conductor pattern 100 is composed of copper. The surface of the copper is plated with tin.

Here, the tin plating of conductor pattern 100 is 0.1-5 μm in thickness, and the height of bump 102 is 5-50 μm.

First, as shown in Fig.4B, a resin film 1 is applied

onto the surface of conductive pattern 100 and flexible substrate 101. The material of resin film 1 may use epoxy resin, polyester resin, fluororesin, or any combinations of these. More illustratively, for example, anisotropic conductive film 107 used in the conventional example in Fig.2 with conductive particles 106 removed therefrom can be used. The thickness should be at least 10 μm and set greater than the height of bump 102.

Next, as shown in Fig.4C, bumps 102 of semiconductor chip 103 are pressed, while being heated, against conductor pattern 100 on flexible substrate 101 with the resin film 1 in between. This heating temperature is set at a range within which resin film 1 becomes softened but not cured. Here, the heating temperature was set at about 100°C.

Since the surface of bumps 102 as well as the tin-plated surface of conductor pattern 100 has been roughened because of crystal growth during plating, bumps 102 and conductor pattern 100 are brought into contact with each other penetrating resin film 1 during the above pressing and heating process.

When conductor chip 103 and flexible substrate 101 are electrically connected, necessary electrical tests etc. are implemented. At this stage, the final product assembly has not yet been finished, and the tests are implemented with the electrical connections temporarily completed. In this case, once bumps 102 are made into contact with conductor pattern 100, the connected state continues even through semiconductor chip 103 is not pressed against flexible substrate 101. Still, it is preferable to provide a slight pressure in order to ensure the electrical connection. From the result of these tests, if semiconductor chip 103 turns out to be defective, the semiconductor 103 is removed from the flexible substrate 101.

In the conventional configuration, since it is unavoidable that a defective chip be removed after the formation of alloy layer 104 between bumps 102 and conductor pattern 100, conductor pattern 100 is peeled off altogether when the defective chip is forcibly removed, making it impossible to reuse the substrate. In contrast, in accordance with this embodiment, bumps 102 are only put in contact with, but not connected to, conductor pattern 100, it is possible to easily remove only the defective chip without causing high stress in conductor pattern 100 of the flexible substrate.

As a result of the electrical tests, if no problems are found, semiconductor chip 103 and flexible substrate 101 are pressed together whilst being heated so that bumps 102 and conductor pattern 100 form an alloy layer 104, thus completing a reliable chip-substrate connection, as shown in Fig.4D. Here, the conditions of heating and pressing are the same as in the case of Figs.1A-1D. Specifically, this process is performed at a temperature of 280°C to 600°C, and each bump is about 100 μm square and is pressed with a load of 10 to 60 gf.

When the above alloy layer 104 is formed, resin film 1 also becomes cured. In this way, it is necessary to achieve curing or hardening due to cross-linking in resin film 1 at a high temperature range within which the alloy layer can be formed. Accordingly, a resin film having characteristics of becoming cured at high temperatures is used in this embodiment.

As has been described heretofore, in this embodiment, since the electrical tests are implemented before the previous step shown in Fig.4C, i.e., before forming an alloy layer 104 from bumps 102 of semiconductor chip 103 and conductor pattern 100 of flexible substrate 101, a defective semiconductor chip 103, if found, can be replaced easily so that flexible substrate 101 can be reused. This can reduce waste as compared to the conventional configuration, providing a cost benefit.

Further, because resin film 1 is punched by bumps 102 in the step shown in Fig.4C, bumps 102 have been already covered with resin film 1 in the pressing and heating process for forming an alloy layer shown in Fig. 4D. Therefore, no phenomenon occurs in which tin plating on the surface of conductor pattern 100 gathers toward bumps 102 thereby forming an alloy layer spreading out from the end face of semiconductor chip 103, as mentioned as a problem in the prior art. As a result, it is possible to solve the problem of edge leakage which occurred in the conventional configuration.

When a flexible substrate which having flexibility is used as the substrate as in this embodiment, the substrate may be flexed during production or depending upon the use thereof as shown in Fig.3. This caused edge leakage in the conventional configuration. However, according to this embodiment, this problem can be solved, so that this configuration is suitable, especially, for a flexible substrate etc., which has flexibility.

In this embodiment, in place of using an anisotropic conductive film as described in Fig.2, the electrical connection between semiconductor chip 103 and flexible substrate 101 is made by alloy layer 104, so that it is possible to create reliable electrical connection.

Although gold was used as the material for bumps 102 and tin was used for plating the surface of conductor pattern 100 in the above embodiment, it is also possible to use solder as the material for bumps 102 and gold for plating conductor pattern 100 in a variational embodiment. In this case, the height of bumps 102 is set at 5-100 μm, and the thickness of the gold plating on conductive pattern 100 is preferably 0.05 μm or more. As to the temperature at a step corresponding to Fig.4D, 200-350°C is suitable. The pressure is set at the same as in the above embodiment.

Although flexible substrate 101 consisting of insulating material having conductor pattern 100 formed directly thereon is used as the substrate in the above embodiment, a configuration in which an adhesive layer is provided between the substrate and the pattern can be used. The material for the substrate is not limited as to its flexibility, hard substrates made up of organic materials, or ceramic substrates may be used. Materials which can be used as hard substrates include epoxy,

glass epoxy, polytetrafluoroethylene, phenol resins. Materials which can be used as ceramic substrates include alumina, zirconia, silicon nitride and silicon carbide ceramics.

As described heretofore according to the invention, when a semiconductor chip is judged as defective from the electrical tests etc., only the defective semiconductor chip can be replaced easily so that the substrate itself onto which a semiconductor chip is to be mounted can be reused. Therefore, it is possible to reduce waste as compared to the conventional configuration, thus providing a cost benefit.

Further, the alloy layer formed by the bumps of the semiconductor chip and the conductor pattern of the substrate will not spread out from the end face of the semiconductor chip so that it is possible to eliminate the conventional problem of edge leak where the alloy layer contacts other areas of the pattern etc., or the end of the semiconductor chip itself.

This invention. does not use an anisotropic conductive film, but uses an alloy layer to form electrical connection between the semiconductor chip and the substrate, so that it is possible to create reliable electrical connection.

Claims

1. A semiconductor element/substrate mounting structure of mounting a semiconductor element having bumps onto a conductor portion of a substrate via the bumps,
characterized in that the bumps are alloyed so as to be integrated to the conductive portion on the substrate, the alloyed portion is formed penetrating through a resin film which is disposed so as to cover the substrate containing conductive portion.

2. A semiconductor element/substrate mounting structure according to Claim 1, wherein the substrate is of a flexible type.

3. A semiconductor element/substrate mounting structure according to Claim 1, wherein the resin film has characteristics which causes cross-linking at a temperature range within which the bumps and the conductive portion on the substrate become alloyed.

4. A mounting method of a semiconductor element for mounting a semiconductor element having bumps so that the bumps are connected to a conductor portion of a substrate, comprising:

a first step of covering a resin film over the substrate together with the conductive portion;
a second step of pressing and heating so that the bumps penetrate through the resin film to come into contact with the conductive portion: and
a third step of pressing and heating so that the bumps and the conductive portion become alloyed between the semiconductor element and the substrate.

5. A mounting method of a semiconductor element according to Claim 4, wherein the substrate is of a flexible type.

6. A mounting method of a semiconductor element according to Claim 4, wherein the resin film has such a characteristic that no cross-linking reaction occurs during the second step and a cross-linking reaction occurs to cure the resin film during the third step.

7. A mounting method according to any of Claims 4 to 6. including electrically testing the semiconductor element between the second and third steps.

8. A mounting method according to Claim 7, wherein said electrical testing is carried out via the contact between at least one of said bumps and the conductor portion.

9. A mounting method according to any of Claims 4 to 8, wherein the temperature to which the resin film is heated is higher in said third step than in said second step.

10. A method of mounting a semiconductor element having electrically conductive contact bumps onto a substrate so as to electrically connect said bumps by alloying to a conductor portion of the substrate,
characterised in that before performing a step of alloying the bumps to the conductor portion, said bumps are preliminarily brought into non-alloyed electrical contact with said conductor portion and electrical testing of the semiconductor element is carried out while maintaining said non-alloyed electrical contact.

11. A method of mounting a semiconductor element having electrically conductive contact bumps onto a substrate so as to electrically connect said bumps by alloying to a conductor portion of the substrate,
characterised in that the method includes
applying a resin film onto a part of the substrate including said conductor portion, and pressing the semiconductor element onto the substrate and heating so that the bumps penetrate through the resin film so as to reach and alloy with the conductor portion.

12. A method according to Claim 11, wherein said bumps are first brought into non-alloyed contact

with the conductor portion, and an alloying step is then carried out.

13. A method according to Claim 12, wherein the resin film is softened during the pressing step so as to facilitate the penetration, and is cured during said alloying step.

FIG.1A
PRIOR ART

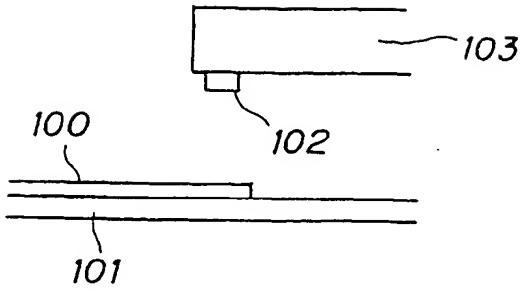


FIG.1B
PRIOR ART

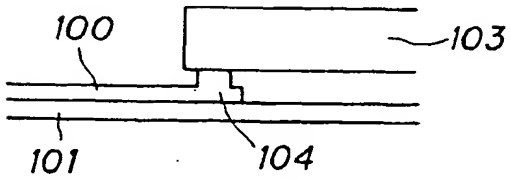


FIG.1C
PRIOR ART

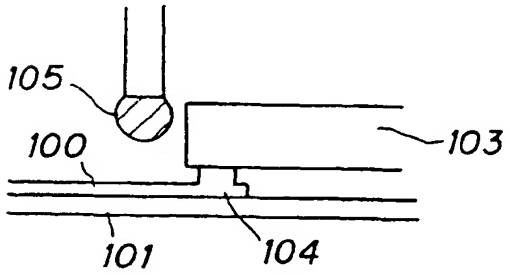


FIG.1D
PRIOR ART

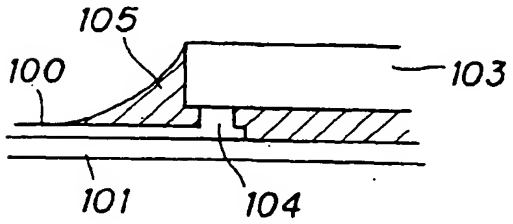


FIG.2
PRIOR ART

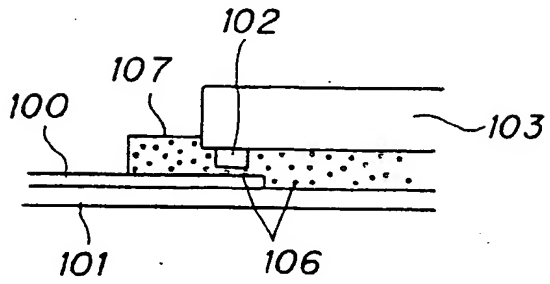


FIG.3
PRIOR ART

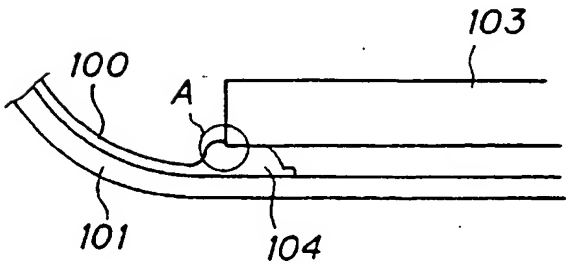


FIG.4A

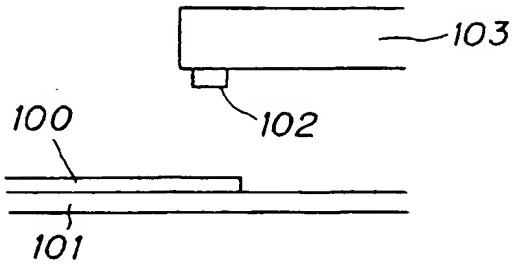


FIG.4B

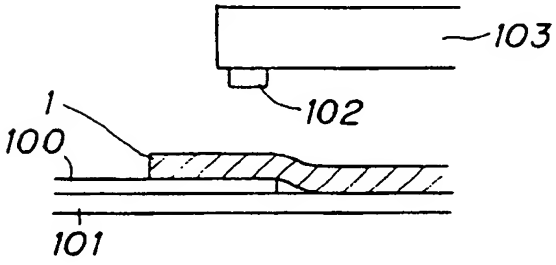


FIG.4C

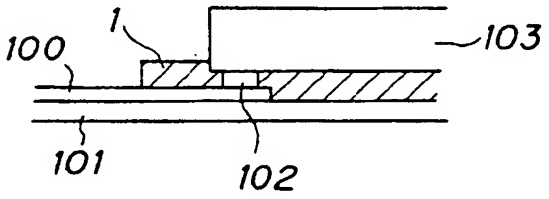
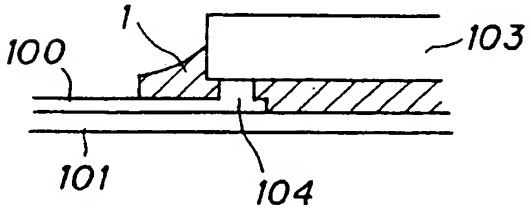


FIG.4D



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(54) A structure of mounting a semiconductor element onto a substrate and a mounting method thereof

(57) A semiconductor element/substrate mounting structure is formed by a first step of covering a resin film (1) over the substrate (101) together with a conductive portion (100); a second step of pressing and heating so that bumps (102) penetrate through the resin film to come into contact with the conductive portion; and a third step of pressing and heating so that the bumps and the conductive portion become alloyed between the semiconductor element (103) and the substrate.

FIG. 4A

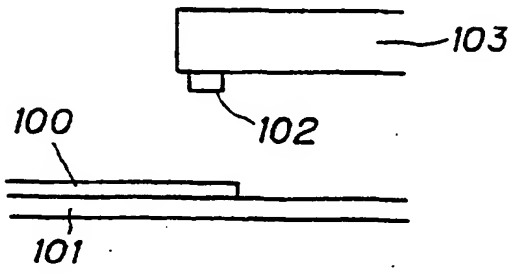

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FIG.4B

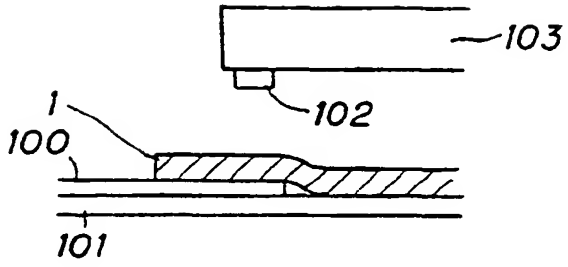


FIG.4C

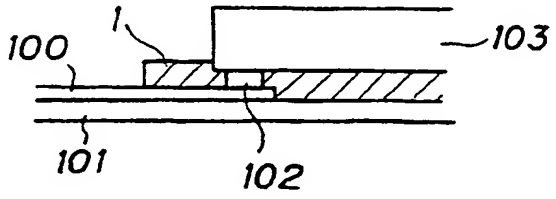
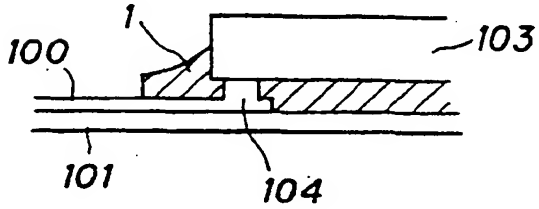


FIG.4D



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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 5608

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THE HAGUE	1 October 1999	Kirkwood, J

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